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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/038,354	01/04/2002	Peter Schuler	112153.125	7032

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10/31/2005

Peter M. Dichiaro
Hale and Dorr LLP
60 State Street
Boston, MA 02109

EXAMINER

LESNIEWSKI, VICTOR D

ART UNIT

PAPER NUMBER

2152

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/038,354	Applicant(s) SCHULTER ET AL.	
	Examiner Victor Lesniewski	Art Unit 2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>7/25/2003</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The amendment filed 8/5/2005 has been placed of record in the file.
2. Claims 1 and 5 have been amended.
3. Claims 9 and 10 have been added.
4. Claims 1-10 are now pending.
5. The applicant's arguments with respect to claims 1-8 have been considered but are moot in view of the following new grounds of rejection.

Information Disclosure Statement

6. The IDS filed 7/25/2003 has been considered.

Response to Amendment

7. The independent claims have been amended to include more details that deal generally with an ARP request between a first and a second processor node and with ARP tables at each node. Also, the amended claims now include a showing of communication between the nodes that avoids the switch node. The amendment proves a change in scope to the independent claims as the independent claims now explicitly state, inter alia, that the first and second processor nodes communicate directly between processor nodes over the non-Ethernet physical network, avoiding the switch node. However, none of the amended claims show a patentable distinction over the prior art as evidenced by the following new grounds of rejection.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. Claims 1, 2, 4-6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox et al. (U.S. Patent Number 6,189,041), hereinafter referred to as Cox, in view of Plummer (RFC 826, "An Ethernet Address Resolution Protocol").

10. Cox disclosed a method by which an Emulated LAN subnetwork attached client in an ATM network can send data to a destination LAN Emulation client on a different ISO layer-3 subnetwork via a data-direct Virtual Channel Connection. The method makes use of Address Resolution Protocol. In an analogous art, Plummer disclosed a description of Address Resolution Protocol.

11. Concerning claims 1 and 5, Cox did not explicitly state the use of ARP tables in the processor nodes to associate IP addresses with the interfaces. However, Cox does associate IP addresses with the interfaces and the use of tables in ARP was well known in the art as evidenced by Plummer whose disclosure shows how ARP uses tables or mappings at each node to track associations between addresses and interfaces. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the system of Cox by adding the ability for each processor node to have its ARP table programmed to associate the IP address of the other node with the corresponding virtual interface as provided by Plummer. Here the combination satisfies the need for an NHRP client in an ELAN IP subnetwork that may

bypass one or more hops by establishing a direct layer-2 connection between the NHRP client and another emulated LAN destination. See Cox, column 4, lines 10-25. This rationale also applies to those dependent claims utilizing the same combination.

12. Some claims will be discussed together. Those claims which are essentially the same except that they set forth the claimed invention as a system are rejected under the same rationale applied to the described claim.

13. Thereby, the combination of Cox and Plummer discloses:

- <Claims 1 and 5>

A method of implementing the address resolution protocol (ARP) in a computing platform having a plurality of processors interconnected by a non-Ethernet physical network, comprising: defining a topology of an Ethernet network to be emulated on the computing platform, the topology including processor nodes and a switch node (Cox, column 2, line 55 through column 3, line 3); assigning a set of processors from the plurality to be processors to act as the processor nodes (Cox, column 6, lines 54-59 and figure 3); assigning a processor to act as the switch node and to emulate an Ethernet switch (Cox, column 7, lines 7-15); allocating virtual interfaces for the underlying non-Ethernet physical network, the virtual interfaces providing direct software communication paths between two processors connected to the non-Ethernet physical network, wherein each virtual interface has a corresponding identification (Cox, column 7, lines 23-36); a first processor node, in response to needing to communicate an IP packet to a target IP node for which the first processor node has an IP address but insufficient, corresponding lower layer address information, communicating an ARP

request to the switch node via the non-Ethernet physical network, wherein the ARP request includes an IP address for the target node (Cox, column 7, lines 37-56); the switch node communicating, via the non-Ethernet physical network, the ARP request to all other processor nodes in the emulated Ethernet network (Cox, column 7, lines 49-56); a second processor node that is assigned the IP address for the target IP node receiving the ARP request and issuing an ARP reply in response (Cox, column 7, lines 56-62); the second processor node having its ARP table programmed to associate the IP address of the first node with a corresponding virtual interface for the underlying non-Ethernet physical network (Plummer, page 7, "An Example," paragraph 2); the first processor receiving and processing the ARP reply (Cox, column 7, line 62 through column 8, line 8); the first processor node having its ARP table programmed to associate the IP address of the target IP node with a corresponding virtual interface for the underlying non-Ethernet physical network (Plummer, page 7, "An Example," paragraph 3); wherein for subsequent unicast IP communication between the first and second nodes, the first and second processor nodes respectively use their ARP tables and the virtual interfaces associated therewith to communicate directly between processor nodes over the non-Ethernet physical network, avoiding the switch node (Cox, column 7, line 62 through column 8, line 8).

- <Claims 2 and 6>

The method of claim 1 wherein the underlying physical network is a point-to-point mesh connecting the plurality of processors (Cox, figure 3).

- <Claims 4 and 8>

The method of claim 1 wherein the switch node is in communication with an external IP network, and wherein the act of communicating an ARP reply includes identifying that the ARP reply is from a processor node in the platform (Cox, column 3, lines 21-35).

- <Claim 9>

The method of claim 1 wherein the second processor node includes driver logic to modify the ARP request to include virtual interface information so that the ARP table of the second processor node associates the IP address of the first node with virtual interface information for the first processor node (Plummer, page 7, "An Example," paragraph 2 and Cox, column 7, lines 1-6).

- <Claim 10>

The method of claim 1 wherein the first processor node includes driver logic to modify the ARP reply to include virtual interface information so that the ARP table of the first processor node associates the IP address of the second node with virtual interface information for the second processor node (Plummer, page 7, "An Example," paragraph 3 and Cox, column 7, lines 52-62).

Since the combination of Cox and Plummer discloses all of the above limitations, claims 1, 2, 4-6, and 8-10 are rejected.

14. Claims 3 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox in view of Plummer, as applied above, further in view of Aditya (U.S. Patent Number 5,918,021).

15. The combination of Cox and Plummer disclosed a method by which an Emulated LAN subnetwork attached client in an ATM network can send data to a destination LAN Emulation client on a different ISO layer-3 subnetwork via a data-direct Virtual Channel Connection. In an analogous art, Aditya disclosed a communication system with a plurality of nodes in which one node is implemented to follow a load balancing scheme.

16. Concerning claims 3 and 7, the combination of Cox and Plummer did not explicitly state the use of one of the processors in a cluster as a load balancing processor. However, this feature is evidenced by Aditya who states the use of a load balancing processor to aid in distributing data traffic among multiple communication channels. It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the combination of Cox and Plummer by adding the ability to use one of the processors in a cluster as a load balancing processor as provided by Aditya. Again the combination satisfies the need for effectuating a method so that a client in an ELAN IP subnetwork may bypass one or more hops by establishing a direct layer-2 connection between the client and another emulated LAN destination. See Cox, column 4, lines 10-25.

17. Thereby, the combination of Cox, Plummer, and Aditya discloses:

- <Claims 3 and 7>

The method of claim 1 wherein a subset of the processors are organized as a cluster and wherein one of the processors in the cluster is a load balancing processor node, and wherein, when any processor in the cluster issues an ARP request, the switch node modifies the ARP reply to include the virtual interface identification for the load

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balancing processor node (Aditya, column 5, line 61 through column 6, line 23 and Cox, column 7, lines 59-62).

Since the combination of Cox, Plummer, and Aditya discloses all of the above limitations, claims 3 and 7 are rejected.

Conclusion

18. The prior art made of record and not relied upon is considered pertinent to the applicant's disclosure.

- Karapetkov et al. (U.S. Patent Number 5,974,452) disclosed a method for determining a destination ATM address in reply to an address resolution inquiry from a source LAN emulation client of a first ELAN.
- Natanson et al. (U.S. Patent Number 6,546,015) disclosed a forwarding engine adapted to assemble Ethernet frames from ATM cells and to segment Ethernet frames back to ATM cells in order to distribute traffic to LAN emulation clients.

19. The applicant's amendment necessitated the new grounds of rejection presented in this office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). The applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

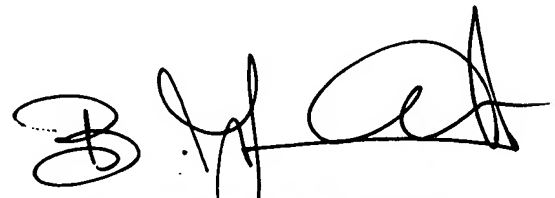
20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor Lesniewski whose telephone number is 571-272-3987. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on 571-272-3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Victor Lesniewski
Patent Examiner
Group Art Unit 2152



BUNJOB JAROENCHONWANIT
PRIMARY EXAMINER